A Circuit-Fed Tile-Approach Configuration for Millimeter-Wave Spatial Power Combining

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***Abstract*—In this paper, a circuit-fed spatially combined transmitter array is described for operation at 44 GHz. The array contains 256 elements where each element consists of a monolithic-microwave integrated-circuit amplifier and a circularly polarized microstrip patch antenna. The array is constructed using 16-element tile-approach subarrays. Each subarray is a two RF-level (three-dimensional) multichip module containing integrated microstrip patch antennas. The basic construction of the transmitter array resembles tile-approach phased arrays; however, the implementation has been tailored for the power-combining application. The peak performance at 43.5 GHz is equivalent isotropic radiated power of 40.6 dBW (11 570 W), effective transmitted power (P_{eff}) of 5.9 W, dc-to-RF efficiency of 7.3%, and system gain of 35 dB.**

***Index Terms*—Active antenna arrays, spatial power combining.**

I. Introduction

SPATIAL and quasi-optical power-combined amplifiers offer the possibility of efficiently combining the output power from a large number of solid-state devices (diodes, transistors, or monolithic-microwave integrated-circuit (MMIC) amplifiers) at millimeter-wave frequencies [1], [2]. In these techniques, the output powers are combined in free space. This is fundamentally different from combining the output powers in a circuit structure, as is done in traditional millimeter-wave amplifiers. The resistive losses in the circuit structure reduces the combining efficiency as larger numbers of devices are combined to achieve higher overall output powers.

A number of spatial power-combining techniques have been explored in recent years. These techniques can be grouped into two broad classes. The first is referred to as the grid approach and is characterized by a repetitive structure of circuit traces and solid-state devices with a unit cell smaller than $\lambda_O/2$ [3], [4]. The circuit traces serve as the receiving antenna, transmitting antenna, and transmission line between active devices. The interaction of the components in this tightly integrated grid is complex [5], [6].

The second broad class of spatial power-combined arrays uses antenna elements spaced $\lambda_O/2$ to λ_O and uses solid-state devices that can be modeled as standalone components. A number of techniques to distribute the input signal to the solid-state devices have been explored. Spatial distribution techniques have been used resembling the general architecture of a space-fed radar array [7]. The mode structure inside a metal waveguide has recently been used with good success [8], [9]. In this paper, a more conventional circuit-fed approach is explored. There are two primary advantages of the circuit-fed approach. First, it provides uniform phase and amplitude input signal to the solid-state devices. Second, it permits adding driver amplifiers in the distribution network, allowing scaling to arbitrarily large arrays and providing high overall system gain without the need for high-output power driver amplifiers.

The other unique aspect of this study is the packaging of the components in the multichip module, including the integration of the patch antenna for operation in the millimeter-wave region. There are two distinct RF layers in the package. A modified load–pull technique has been developed to compensate for the signal discontinuity in the layer-to-layer transition.

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II. Array Configuration

A spatial power-combined transmitter array has been constructed for operation in the 43.5–45.5-GHz band. The array contains 256 elements, where each element consists of a MMIC amplifier and a circularly polarized microstrip patch antenna. The array is constructed using 16-element tile-approach subarrays. In the final realization of the array, the feed network produces 16 coax-blindmate connectors that mate to 16 subarrays. The basic construction of the transmitter array resembles tile-approach phased arrays; however, since the array is not electrically scanned, there are no phase shifters and the element spacing has been increased to $0.8\lambda_0$. Further, a low thermal resistance path is provided from the attachment point of the MMICs to the cooling fins.

A. Feed Network

In this study, the input feed network was realized using five individually packaged 1-to-4 power dividers and coaxial cable. The coaxial feed network was chosen for its relative ease of construction. It can be seen in the photograph of the transmitter array shown in Fig. 1. A 2-dBm input signal is required at the 2.4-mm connector at the base of the transmitter. This is the input to the first 1-to-4 power divider. The four outputs of the first power divider are connected to four additional 1-to-4 power dividers. The 16 outputs from the second level of power dividing are run to 2.4-mm blind-mate connectors in the array base plate.

The task of the feed network is to provide an input signal at 14 dBm and appropriate phase to the inputs of each of the subarrays. This requires the feed network to have driver amplifiers to boost the signal level and to overcome the fan-out and line losses of the feed. In addition, the feed network needs the ability to adjust the amplitude and phase of each of the output signal. This is required to overcome the imperfections in construction

Fig. 1. Photograph of the 256-element array.

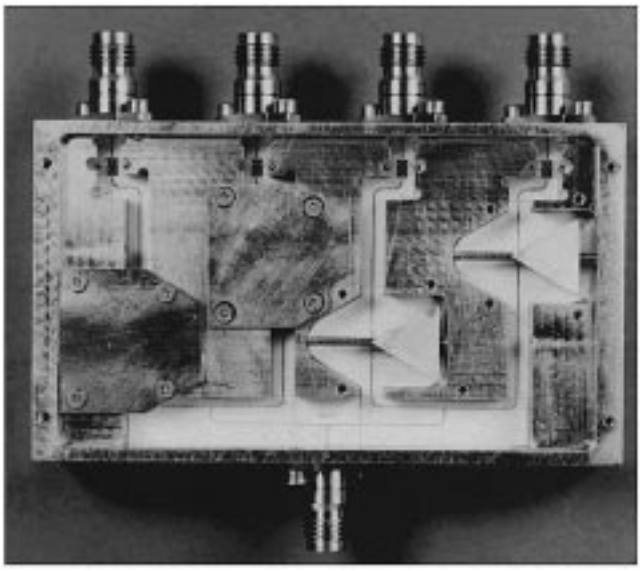

Fig. 2. Photograph of the 1-to-4 power divider.

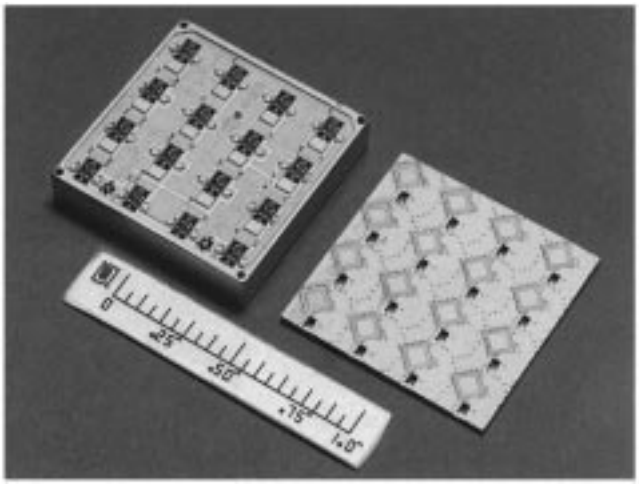

Fig. 3. Photograph of the 16-element subarray.

of the feed network and the variations in the MMICs used as driver amplifiers. Further, as described below, the subarrays are populated with MMICs that have similar output phase, but the output phase varies from subarray to subarray and must be compensated.

The RF circuitry of the 1-to-4 power divider is shown in Fig. 2. The RF circuitry is constructed on 0.125-mm (5-mil) alumina, and two levels of Wilkinson power dividers are used to divide the signal into four paths. This device contains a driver amplifier near the connector in each of the four output ports. The gate bias circuit for each of the driver amplifiers contains a precision potentiometer to equalize the output power at each port. The phase of the RF signal can also be adjusted for each port by using the dielectric overlay visible at the center of the power divider in the right two signal channels. The overlay is a three layer construction of Duriod 6010–copper–Duriod 6010. A tapped hole passes through the center copper section of the wedge so that the position of the wedge relative to the microstrip line can be adjusted by turning the lead screw. The Duriod layer resting on top of the microstrip line changes the effective dielectric constant and, hence, the phase delay through the microstrip line [10]. The dielectric overlay requires intimate contact with the microstrip line for proper operation. The metal cover plate, visible in the left two channels, provides the contact pressure. The Teflon in the Duriod material reduces the friction between the wedge and alumina substrate below and the metal cover plate above. No lubricant was required. The nominal gain through the power divider is +4 dB and the phase tuning range is approximately 250°.

B. Subarray Design

The details of a breadboard version of the subarray package were reported in [11]. In the current configuration, the size of the subarray has been reduced so that it can be tiled into the extended array and maintain the 0.8-λ_O spacing between elements in adjacent subarrays. The main difference in this version of the subarray is that there is a common gate and common drain bias bus. This permits the connector count to be reduced to three: a blind-mate connector for the RF signal and two glass bead pins for the bias voltages. A photograph of the subarray is shown in Fig. 3. The subarray contains two RF layers. The lower RF layer is standard hybrid circuit constructed on 0.125-mm alumina. It contains a 1-to-16 power divider and the the dc-bias circuitry. The 16 MMIC amplifiers are also placed in holes in the alumina board, enabling the MMICs to be silver epoxied directly to the Cu-W subarray carrier. The MMIC amplifiers are measured and placed into bins with phase difference less than 20° and output power variation less than 1 dB. When constructing a subarray, MMICs from a single bin are taken to reduce the phase and amplitude variations among the subarray elements.

The antenna layer is constructed with a three-layer Duriod 6002 printed circuit board. The signal at the output of the MMIC

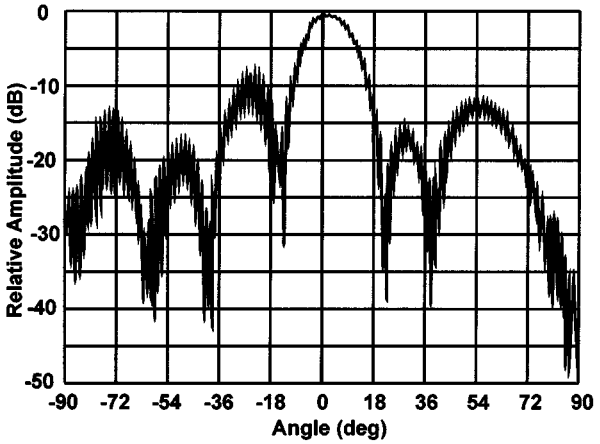

Fig. 4. Spinning linear radiation power of a typical 16-element subarray.

amplifier is connected by a 75-μm-wide ribbon bond to the antenna layer. Just after the ribbon bond attachment site, the signal transitions to asymmetric stripline, where it encounters a reactive T-junction before feeding the circularly polarized cavity-backed patch antenna. Details on the cavity-backed patch antenna can be found in [12].

The discontinuity of the ribbon bond that routes the signal from the MMIC layer to the antenna layer is compensated by using a load–pull technique. A test device is constructed that contains a representative MMIC amplifier, the ribbon bond transition, and a length of asymmetric stripline. Appropriate thru-reflect-line (TRL) calibration standards are designed to place a vector network analyzer reference plane in the asymmetric stripline a few hundred micrometers from the ribbon bond. The load impedance presented at the reference plane is varied while the output power and power-added efficiency (PAE) of the MMIC are monitored. By constructing contour plots of the output power and PAE overlaid on a Smith chart for the corresponding impedance at the reference plan, it is readily ascertained what impedance should be presented at the reference plane. With this information, an impedance transformer can be designed.

III. Measurements

Transmitter arrays with 8 and 16 subarrays were constructed and measured. In addition, the subarrays were fully characterized before inserting them into the array.

The subarrays were characterized by measuring their far-field radiation patterns and their equivalent isotropic radiated power (EIRP). Fig. 4 shows the spinning linear pattern for a subarray at 44.5 GHz. The main beam and null-beamwidth are slightly wider than what is predicted from theory for a uniform array. The amplitude of the sidelobes are uneven and vary several decibels from theory. These two factors indicate that there are phase and amplitude imbalances in the subarray. Following the procedure described in [13], the effective radiated power is measured, and the effective transmitted power, dc-RF efficiency, and combining efficiency are calculated for the subarrays. The available power in this study was found by summing the output power of the MMICs measured using a wafer prober before inserting them into the subarrays. These results are summarized in Table I.

TABLE I
Performance Summary of the two Arrays

	Subarrays		128 Element Array		256 Element Array	
	Peak	Avg	Peak	Avg	Peak	Avg
EIRP (dBW)	17.9	17.1	35.9	35.3	40.7	40.1
P_{eff}	0.50 W	0.42W	3.8 W	3.3 W	5.9 W	5.0 W
$\eta_{dc\text{-}RF}$	10.3%	7.6%	8.2%	7.1%	6.8%	5.8%
η_{comb}	50.7%	41.8%	47.5%	41.5%	39.2%	32.3%

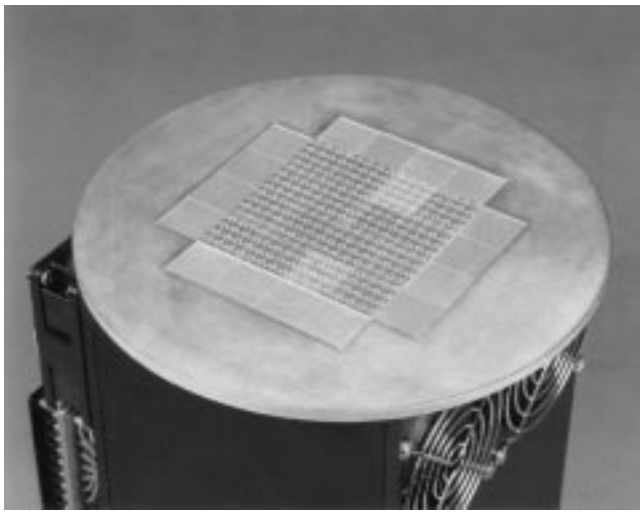

Fig. 5. Face of the 256-element array.

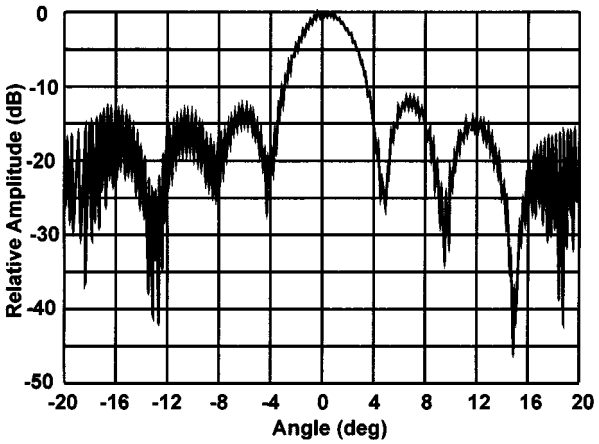

Fig. 6. Spinning linear radiation power of the 256-element array at 44 GHz.

Two versions of the transmitter array where constructed. The first containing 128 elements (eight subarrays) and the second containing 256 elements (16 subarrays). A photograph of the face of the 256-element array is shown in Fig. 5. The variations in the output phase of the subarrays is equalized by turning the subarrays on individually and adjusting the phase trim device in the corresponding 1-to-4 power divider so that all of the received signals at the standard gain horn in the far field of the array have the same phase. The phase is adjusted at a frequency of 44.5 GHz (center band). The measured spinning linear far-field

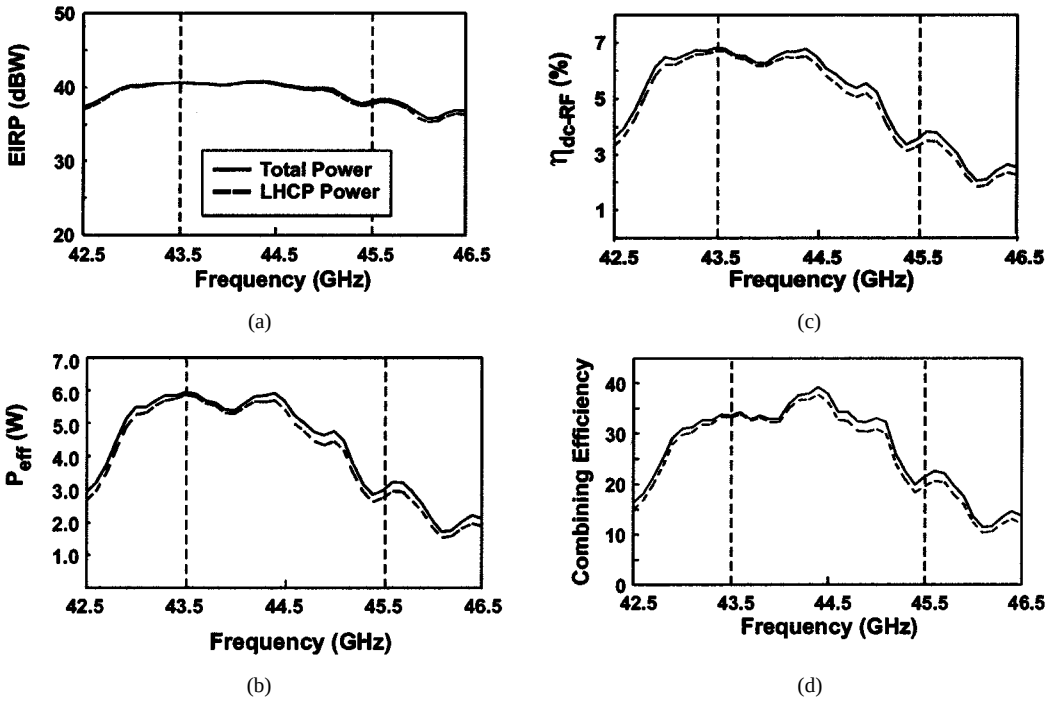

Fig. 7. (a) Measured EIRP versus frequency for the 256-element array. (b) Effective transmitted power versus frequency for the 256-element array. (c) DC–RF efficiency versus frequency for the 256-element array. (d) Combining efficiency versus frequency for the 256-element array.

pattern is shown in Fig. 6. Note that the scale of the abscissa, the degrees axis, only extends from -20° to $+20^{\circ}$. The main beam and null beamwidth are again slightly wider than for a uniform array. Note, however, the sidelobe amplitudes are more uniform and close to that expected from theory, indicating that the distribution of the phase and amplitude variations among the array elements is more uniform. The measured EIRP and calculated effective transmitted power, dc-RF efficiency, and combining efficiency are shown in Fig. 7(a)–(d). The peak and average values across the 43.5–45.5-GHz range for these figures-of-merit are given in Table I.

The combining efficiency is the most revealing of the figures-of-merit reported here because it best quantifies how well the array is constructed. In addition, it serves as a convenient way to estimate the output power of the array based on the number and output power of the individual solid-state devices in the array. A fundamental premise of the spatial power-combining technique is that the combining efficiency will remain constant independent of the number of elements in the array. From Table I, it is seen that this holds for the 128-element array. The average combining efficiency of the individual subarrays is 41.8%, and the combining efficiency of the 128-element array is 41.5%. However, the combining efficiency of the 256-element array decreases to 32.3%.

A series of measurements was performed to investigate this decrease in combining efficiency. Measurements of the combining efficiency as a function of frequency revealed that the average subarray combining efficiency equaled the 256-element array combining efficiency at center band. This is the frequency where the phase trim devices where adjusted for no phase variation among the subarray's output signal. However, at other frequencies in the band of interest, the phase variation among the

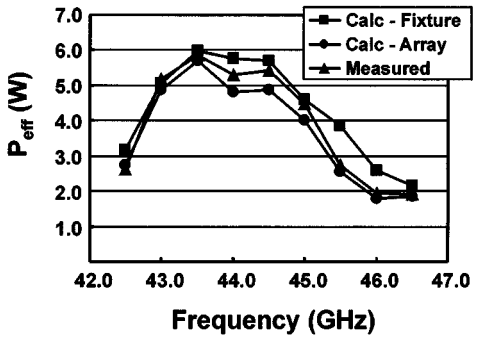

Fig. 8. Calculated and measured combining efficiency accounting for phase and amplitude variations for the 256-element array.

subarray's output signal where significant, leading to a significant decrease in combining efficiency. The problem was traced to voltage standing-wave ratio (VSWR) effects in the feed network between the two levels of 1-to-4 active power dividers. Note that, in the 128-element array, there was only one level of the 1-to-4 active power dividers.

As a final check, the effective transmitted power of the 256-element was calculated as a function of frequency accounting for the phase and amplitude variations in the subarrays. The phase variations where measured by turning the subarrays on one at a time in the 256-element array configuration. The amplitude variations were measured in two ways. The first was in the array configuration, and the second was from the measurements of the subarrays individually in the one-subarray test fixture. The plot in Fig. 8 compares the calculated and measured effective transmitted power. The measured effective transmitted power is bracketed by the results of the two different calculated transmitted powers. This indicates that problem lies in the design of

the input signal distribution network and that, as expected, the combining efficiency of the subarrays is unchanged as they are used in larger arrays.

IV. Summary

This paper has described the results of an investigation on a circuit-fed tile-approach spatial power-combined array. Two unique features of the array are the use of the circuit-fed technique and the packaging technique of the array. The performance of the array has been well characterized, with particular attention paid to the combining efficiency. It has been shown that the spatial power-combining technique provides a method to maintain constant combining efficiency of the MMIC devices as more and more devices are used.

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Sean M. Duffy, photograph and biography not available at time of publication.